Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 [CURRENTLY AMENDED] A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each including a control electrode and a path switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) on and off while the voltage source has the first level and (b) off and on while the voltage source has the second level, [[and]] said circuitry including at least one voltage responsive switchable capacitor connected between the first terminal and the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the first and second levels, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels.

Claim 2 CANCELED

Claim 3 [CURRENTLY AMENDED] The circuit of claim [[2]] 1 wherein the at least one switchable capacitor is connected between one of the control electrodes and a DC power supply terminal of the circuit.

Claim 4 [CURRENTLY AMENDED]The circuit of claim 3 wherein the circuitry further ~~including~~ includes a resistive element connected to supply current to the at least one switchable capacitor in response to the voltage at the [[input]] first terminal.

Claim 5 [CURRENTLY AMENDED] The circuit of claim [[4]] 1 wherein said first and second transistors are respectively a PFET and an NFET and said at least one switchable capacitor comprises a PFET field effect transistor having a first electrode connected to a gate electrode of the NFET second transistor and a second electrode connected to a power supply terminal for supplying current to the PFET second transistor source drain path while the PFET second transistor source drain path is on.

Claim 6 [CURRENTLY AMENDED] The circuit of claim 5 wherein said resistive element, PFET, NFET and said at least one switchable capacitor are included on an integrated circuit chip, and said resistive element comprises a resistor.

Claim 7 [CURRENTLY AMENDED] The circuit of claim [[2]] 1 wherein said first and second transistors are respectively a PFET and an NFET and said at least one switchable capacitor comprises [[a]] an NFET field effect transistor having an electrode connected to a gate electrode of the PFET first transistor and a second electrode connected to the power supply terminal for supplying current to the NFET second transistor source drain path while the NFET second transistor source drain path is on.

Claim 8 [CURRENTLY AMENDED] The circuit of claim 1 wherein the at least one capacitor includes first and second voltage controllable ~~switched~~ switchable capacitors respectively connected to delay coupling of the transitions to the control electrodes of the first and second transistors.

Claim 9 (Previously Presented) The circuit of claim 8 wherein said first and second capacitors are respectively connected between the control electrodes of the first and second transistors and first and second power supply terminals of the circuit and are such that (a) the first capacitor is arranged to have a finite capacitance value on a first side of a first voltage threshold and a substantially open circuit on a second side of the first threshold, and (b) the second capacitor is arranged to have a finite capacitance value on a second side of a second voltage threshold and a substantially open circuit on a first side of the second threshold, the first and second thresholds differing from each other and being between the first and second levels.

Claim 10 CANCELED

Claim 11 [CURRENTLY AMENDED]The circuit of claim 9 wherein the circuitry further ~~including~~ includes first and second resistive elements respectively connected to supply current to the first and second capacitors in response to the voltage at the first terminal.

Claim 12 (Previously Presented) The circuit of claim 11 wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET.

Claim 13 (Previously Presented) The circuit of claim 12 wherein the first and second transistors, the first and second resistive elements, and the first and second capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

Claim 14 [CURRENTLY AMENDED]The circuit of claim 8 wherein the circuitry further ~~including~~ includes first and second inverters each having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor.

Claim 15 (Original) The circuit of claim 14 wherein the first and second transistors are field effect transistors, the first and second inverters comprise field effect transistors, and the first and second capacitors comprise field effect devices.

Claim 16 (Previously Presented) The circuit of claim 15 wherein all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second field effect transistors and the first and second inverters.

Claim 17 (Original) The circuit of claim 16 wherein the first and second resistors are respectively included in the first and second inverters.

Claim 18 [CURRENTLY AMENDED] The circuit of claim 17 wherein the first and second transistors are respectively a PFET and an NFET, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the [[input]] first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof.

Claim 19 (Original) The circuit of claim 18 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, the second resistor being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

Claim 20 (Original) The circuit of claim 19 wherein the first and second capacitors respectively include an NFET and a PFET.

Claim 21 (Original) The circuit of claim 20 wherein the NFET and PFET included in the first and second capacitors respectively have different first and second thresholds between the first and second levels, the NFET included in the first capacitor having a finite capacitance value for voltages below the first threshold and being a substantially open circuit for voltages greater than the first threshold, the PFET included in the second capacitor having a finite capacitance value for voltages greater than the second threshold and being a substantially open circuit for voltages less than the second threshold, the first threshold being greater than the second threshold.

Claim 22 (Previously Presented) A method of operating a driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite first and second power supply terminals, an output terminal between the series connected paths, first and second switchable capacitors respectively connected between the control electrodes and the first and second power supply terminals, the method comprising: during a first interval: turning on and off the paths of the first and second transistors, respectively, while the second capacitor is charged and the first capacitor is switched off by applying (a) a first voltage having a first value to the control electrode

of the first transistor, (b) the first voltage value across the second capacitor, and (c) a second voltage having the first value to the control electrode of the second transistor; during a second interval: turning off and on the paths of the first and second transistors, respectively, while the second capacitor is switched off and the first capacitor is charged by applying (a) the second value of the first voltage to the control electrode of the first transistor, (b) the first voltage value across the first capacitor, and (c) the second value of the second voltage to the control electrode of the second transistor; during an initial portion of a first transitional period between the first and second intervals: turning off the path of the first transistor while maintaining the path of the second transistor off by changing the first voltage from the first value toward the second value while the first capacitor remains turned off and the second capacitor is charged; during a second portion of the first transitional period turning on the path of the second transistor while maintaining the path of the first transistor off by changing the charge on the second capacitor so that there is a change in the value of the second voltage from the first value toward the second value; during an initial portion of a second transitional period between the second and first intervals: turning off the path of the second transistor while maintaining the path of the first transistor off by changing the second voltage from the second value toward the first value while the second capacitor remains turned off and the first capacitor is charged; and during a second portion of the second transitional period turning on the path of the first transistor while maintaining the path of the second transistor off by changing the charge on the first capacitor so that there is a change in the value of the first voltage from the second value toward the first value.

Claim 23 (Original) The method of claim 22 further comprising the steps of: switching off the first capacitor during the second portion of the first transitional period prior to the value of the first voltage, as applied to the control electrode of the first transistor, reaching the first value; and switching off the second capacitor during the second portion of the second transitional period prior to the value of the second voltage, as applied to the control electrode of the first transistor, reaching the second value.

Claim 24 (Original) The method of claim 23 wherein the first and second capacitors are switched on and off in response to the first and second voltages having values on opposite sides of first and second thresholds respectively associated with the first and second capacitors.